Simulation of Trapping Effects in 4H-Silicon Carbide Metal Semiconductor Field Effect Transistor (4H-SiC MESFET)

Suman Kumar

Department of Electronics & communication Engineering

National Institute of Technology

Rourkela, 769008

(2009-2011)

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A THESIS

SUBMITTED IN PARTIAL FULFILLMENT OF THE

REQUIREMENTS FOR THE DEGREE OF

Master of Technology

In

V.L.S.I & EMBEDDED SYSTEM

By

Suman Kumar

Roll No. – 209EC2128

Under the Guidance of

Dr. N.V.L.N.MURTY

Department of Electronics & communication Engineering

National Institute of Technology

Rourkela, 769008

(2009-2011)

National Institute Of Technology
Rourkela

DECLARATION

I hereby declare that this thesis entitled "**Simulation of Trapping Effects in 4H-Silicon Carbide Metal Semiconductor Field Effect Transistor (4H-SiC MESFET)**" submitted to National Institute of Technology, Rourkela for the award of the degree of Master of Technology is a record of original work done by me under the guidance Dr. N.V.L.N. Murty and that it has not been submitted anywhere for any award. Where other sources of information have been used, they have been acknowledged.

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CERTIFICATE

This is to certify that the thesis entitled, **"Simulation of Trapping Effects in 4H-Silicon Carbide Metal Semiconductor Field Effect Transistor (4H-SiC MESFET)"** submitted by **Mr. Suman Kumar** in partial fulfillment of the requirements for the award of Master of Technology Degree in **ELECTRONICS & COMMUNICATION ENGINEERING** with specialization in **"V.L.S.I & EMBEDDED SYSTEM"** at the National Institute of Technology, Rourkela is an authentic work carried out by him under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University / Institute for the award of any Degree or Diploma.

Date

Dr. N.V.L.N. Murty

SUPERVISOR

ACKNOWLEDGEMENT

I would like to extend my gratitude and my sincere thanks to my honorable, esteemed supervisor **Dr. N.V.L.N. Murty,** Department of Electronics & Communication Engineering for the ideas that led to this work, his timely comments, guidance, support and patience throughout the course of this work. He is my source of inspiration. Her trust and support inspired me in the most important moments of making right decisions and I am glad to work under her supervision.

I am very much thankful to our Head of the Department, **Prof. S. K. Patra**, for providing us with best facilities in the department and his timely suggestions. I am very much thankful to all my teachers **Prof. K. K. Mahapatra, Prof. D. P. Achaarya, Prof. G. S. Rath, Prof. S. Meher and Prof. Samit Ari** for providing a solid background for my studies. They have been great sources of inspiration to me and I thank them from the bottom of my heart.

I would like to thank all my friends specially my classmates and senior of VLSI (Mr. Ayashkanta, Mr. P. Karuppanan) for all the thoughtful and mind stimulating discussions we had, which prompted us to think beyond the obvious. I've enjoyed their companionship so much during my stay at NIT, Rourkela. Special thanks go to Mr. Pallab Majhi for appraising my work critically.

Last but not least I would like to thank my parents, who taught me the value of hard work by their own example. They rendered me enormous support being apart during the whole tenure of my stay in NIT Rourkela.

SUMAN KUMAR

M.Tech (V.L.S.I & EMBEDDED SYSTEM)

CONTENTS

ABSTRACT

4H-SiC MESFETs have a huge potential in high-power devices atmicrowave frequencies due to their wide bandgap features of high electric breakdown fieldstrength, high electron saturation velocity and high operating temperature.

A Physics-based analytical model for the static I-V characteristics of 4H-SiC MESFETs on high-purity semi-insulating substrates (HPSI) has been proposed. Unlike the existing analytical models, At first semi-insulating nature of the substrate is modeled by considering single trap concentration and compared with theoretical model without taking any trap. Then it is noted that drain current is reduced by some factor due to trap of electron from channel to substrate. Then S.I 4H-SiC substrate is modeled by considering three dominant intrinsic deep acceptor-like traps responsible for carrier compensation in HPSI 4H-SiC substrates for the first time. To further improve the accuracy, field–dependent mobility of electrons in the linear region and channel-length modulation in saturation region are considered in deriving the static I-V characteristics in addition to the substrate effects. The temperature dependence of carrier trapping and detrapping into/from the multiple deep levels and the corresponding I-V variations is analytically studied. Moreover, this model includes source and drain series resistances which are significant in 4H-SiC due to less low-field mobility of electrons compared to GaAs. Some of the simulated results are compared with the reported experimental results to check the validity of the proposed method. This model may serve as a basis to study complicated trapping phenomenon of multiple traps and the related microwave performance of 4H-SiC MESFETs.

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Notation

symbol	Description	Unit
Z	Channel width	µm
L	Channel Length	µm
a	Channel depth	µm
µ	mobility	$cm^2/v-sec$
q	Magnitude of electronic charge	c
E_c	Bottom of conduction band	eV
E_{fs}	Fermi energy level	eV
E_v	Top of valance band	eV
E_g	Energy band gap	eV
ε	Electric field	V/cm
ε_c	Critical field	V/cm
h	Plank's constant	J-s
k	Boltzmann constant	J/K
m^*	Effective mass	kg
n	Density of free electron	cm^{-3}
N_c	Density of state in conduction band	cm^{-3}
N_v	Density of state in valance band	cm^{-3}
n_i	Intrinsic carrier concentration	cm^{-3}
v_s	Saturation velocity	Cm/sec
v_{th}	Thermal velocity	Cm/sec
V_{bi}	Built in potential	V
ε_s	Semiconductor permittivity	F/cm
T	Absolute Temperature	K
N_A	Acceptor impurity density	cm^{-3}
N_V	Acceptor impurity density	cm^{-3}

Chapter-1

Introduction and scope of Thesis

1.1. Silicon Carbide

Silicon carbide (SiC) is an attractive wide band-gap semiconductor material for high-power, high-voltage, high-frequency and high-temperature applications [1] due to its superior properties, such as the wide bandgap, high critical electric field, high thermal conductivity and high electron.

Silicon carbide (SiC) is a very promising material for use in high performance semiconductor devices. Among the most important transport parameters for electronic devices are the mobility (μ), saturation velocity (v_{sat}), breakdown electric field (E_{crit}), and thermal conductivity (λ). The mobility describes the mean velocity that the electrons and holes travel with when an electric field is applied. At low electric fields the velocity increases proportional to the field. At higher fields the proportionality is lost and the velocity is saturated at v_{sat}.

When the electric fields exceed E_{crit}, the impact ionization becomes large, rapidly increasing the current, which destroys the material if the current is not limited. The thermal conductivity does not directly affect the performance, but with a good thermal conductivity it is easier to conduct the heat away from the chip to outside. As the mobility and saturation velocity are reduced at high temperatures, a high thermal conductivity indirectly gives better performance for power devices. SiC has developed into one of the leading contenders among the wide bandgap semiconductors.

1.1.1. SiC Polytype

Silicon carbide exists in about hundred of crystalline forms. The polymorphism of SiC is characterized by a large family of similar crystalline structures called polytypes. In which the most common polytypes for electronic devices are 4H-, 6H- and 3C-SiC.

For microwave application the 4H-SiC polytype is preferable because it has a larger bandgap and higher electron mobility than 6H-SiC. It is the wide band gap of 3.2 eV, compared to 1.1 eV for Si and 1.4 eV for GaAs, that gives SiC its major benefit for high power devices. This wide bandgap gives rise to a breakdown electric field that is 10 times higher than in GaAs or Si [2].

1.1.2. General properties of 4H- Silicon Carbide

a. Mobility

At low electric field, the drift velocity (v_d) is proportional to electric field strength (ε) and the proportionality constant is defined as mobility (μ) in $cm^2/v - sec$.

$$V_d = \mu\varepsilon$$

Mobility decreases with effective mass (m^*) and increases with Temperature (T)

$$\mu = (m^*)^{-3/2} . T^{1/2}$$

The mobility is a number that defines how easily the electrons and holes can be moved in an electric field. Due to random scattering within the crystal, the velocity does not increase with constant acceleration as in a vacuum. The electron velocity rather quickly reaches an equilibrium mean-velocity proportional to the mobility and the electric field.

The mobility in SiC is somewhat lower than for silicon and much lower than GaAs. This results in a larger source resistance and lower transconductance than GaAs MESFET [2].

b. Band Gap

Band gap generally refers to the energy difference (in electron volts) between the top of the valence band and the bottom of the conduction band in insulators and semiconductors where no electron states can exist. Without a band-gap the crystal is a metal, and with a large band-gap the crystal is an insulator. A semiconductor has a band-gap up to a few eV. 4H-SiC have large band-gap of 3.2 eV. For such a large band gap the intrinsic carrier concentration is negligible at higher temperature. The intrinsic carrier concentration is responsible for the leakage current and thermal noise.

c. Saturation Velocity

Saturation velocity is the maximum velocity a charge carrier in a semiconductor, generally an electron, attains in the presence of very high electric fields. Saturation velocity is a very important parameter in the design of semiconductor devices, especially field effect transistors, which are basic building blocks of almost all modern integrated circuits. Typical values of saturation velocity may vary greatly for different materials, for example for Si it is in the order of $1 \times 10^7\ cm/s$, for GaAs $1.2 \times 10^7\ cm/s$, while for 4H-SiC, it is near $2 \times 10^7\ cm/s$. A high saturation velocity allows faster devices with smaller switching times.

d. Critical Electric Field

The critical electric field is related to the impact ionization rate, which increases as the carrier energy exceeds the band-gap. Due to the large bandgap the critical electric field is thus about 10 times higher in SiC than for small band-gap materials, such as Si and GaAs. With high

E_{crit} devices can be much smaller for the same voltage, alternatively operate at much higher voltages. A summary of the important parameters of 4H-SiC in comparison to other semiconducting materials Si and GaAs is shown in table 1.1

Property	**Si**	**GaAs**	**4H-SiC**	**GaN**
Bandgap (eV)	1.11	1.43	3.2	3.4
Relative Dielectric constant	11.8	12.8	9.7	9.0
Breakdown Field (V/cm)	6×10^5	6.5×10^5	35×10^5	35×10^5
Saturated velocity (cm/sec)	1×10^7	1×10^7	2×10^7	1.5×10^7
Electron mobility (cm^2/v-sec)	1350	6000	800	1000
Hole mobility (cm^2/v-sec)	450	330	120	300
Thermal conductivity (W/cm-k)	1.5	0.46	4.9	1.7

Table 1 : Comparison of basic material properties of Si, GaAs, 4H-SiC, GaN

1.1.3 Applications of 4H-SiC Electronics

High temperature device operation and high-power device operation are the two useful advantages of SiC-based electronics.

a. High temperature device operation

The wide band gap energy and low intrinsic carrier concentration of 4H-SiC allow 4H-SiC to maintain semiconductor behavior at much higher temperatures than silicon, semiconductor electronic devices function in the temperature range where intrinsic carriers are negligible so that conductivity is controlled by intentionally introduced dopant impurities. As temperature increases, intrinsic carriers increase exponentially so that undesired leakage currents grow

unpredictably large, and eventually at still higher temperatures, the semiconductor device operation is overcome by unrestrained conductivity as intrinsic carriers exceed intended device doping which is discussed in [1, 3].

b. High power device operation

The high breakdown field and high thermal conductivity of 4H-SiC with high temperatures operation theoretically allows for high power operation. 4H-SiC's high breakdown field and wide energy band gap enable much faster power switching devices.

While SiC's smaller on-resistance and faster switching helps minimize energy loss and heat generation, SiC's higher thermal conductivity enables more efficient removal of waste heat energy from the active device. Because heat energy radiation efficiency increases greatly with increasing temperature, 4H-SiC's ability to operate at high junction temperatures allows more efficient cooling to take place, so that heat sinks and other device-cooling hardware (i.e., fan cooling, liquid cooling, air conditioning, etc.) typically needed to keep high-power devices from overheating can be made much smaller or even eliminated [1].

1.1.4. Benefits of high power and high temperature 4H-SiC devices

The operation of high temperature and high power 4H-SiC electronics is very helpful in aerospace systems like jet-aircraft weight savings, reduced maintenance, reduced pollution, higher fuel efficiency, and increased operational reliability. 4H-SiC high-power switching also enable large efficiency gains in electric power management and control. More efficient electric motor drives which will benefit industrial production systems as well as transportation systems such as diesel-electric railroad locomotives, electric mass-transit systems, nuclear-powered ships, and electric automobiles and buses [1].

1.2. Metal-Semiconductor Field Effect Transistor (MESFETs)

The Metal-Semiconductor-Field-Effect-Transistor (MESFET) consists of a conducting channel positioned between a source and drain contact region as shown in the Figure 1.1. The carrier flow from source to drain is controlled by a Schottky metal gate. The control of the channel is obtained by varying the depletion layer width underneath the metal contact which modulates the thickness of the conducting channel and thereby the current between source and drain.

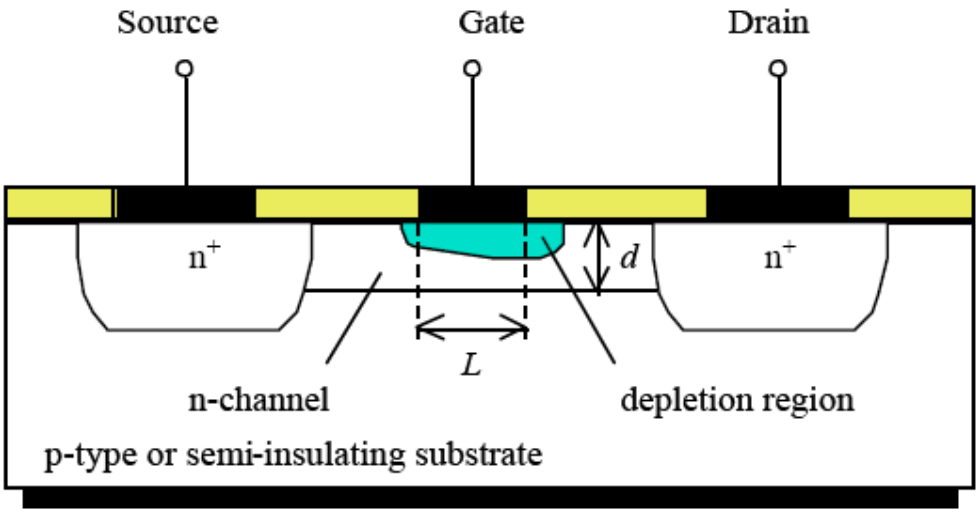

Figure 1.1: Structure of a MESFET with gate length, L, and channel thickness d

The key advantage of the MESFET is the higher mobility of the carriers in the channel as compared to the MOSFET. The higher mobility leads to a higher current, trans-conductance and transit frequency of the device.

The disadvantage of the MESFET structure is the presence of the Schottky metal gate. It limits the forward bias voltage on the gate to the turn-on voltage of the Schottky diode. This turn-on voltage is typically $0.7\,V$ for GaAs Schottky diodes. The threshold voltage therefore

must be lower than this turn-on voltage. As a result it is more difficult to fabricate circuits containing a large number of enhancement-mode MESFET.

The higher transit frequency of the MESFET makes it particularly of interest for microwave circuits. While the advantage of the MESFET provides a superior microwave amplifier or circuit, the limitation by the diode turn-on is easily tolerated. Typically depletion-mode devices are used since they provide a larger current and larger trans-conductance and the circuits contain only a few transistors, so that threshold control is not a limiting factor. The buried channel also yields a better noise performance as trapping and release of carriers into and from surface states and defects is eliminated.

1.2.1. MESFET Principle of Operation

The current-voltage characteristics of a thin n-type 4H-SiC layer in which electrons are carrying the current are plotted in Figure.

This layer is supported by an semi-insulating 4H-SiC substrate. At the surface of the conducting layer, two ohmic contacts are made, called the source and drain. A cross section of this device is shown in Figure 1.2. If a positive voltage V_{ds} is applied to the drain, electrons will flow from source to drain. Hence the source acts as the origin of carriers and the drain as a sink. For small voltages, the 4H-SiC layer behaves like a linear resistor. For bigger voltages, the electron drift velocity does not increase at the same rate as the electric field E. As a result, the current-voltage characteristic falls below the initial resistor line. As V_{ds} is further increased, E reaches a critical field, E_c for which the electrons reach a maximum velocity v_s. At this drain voltage, the current starts to saturate [4, 5].

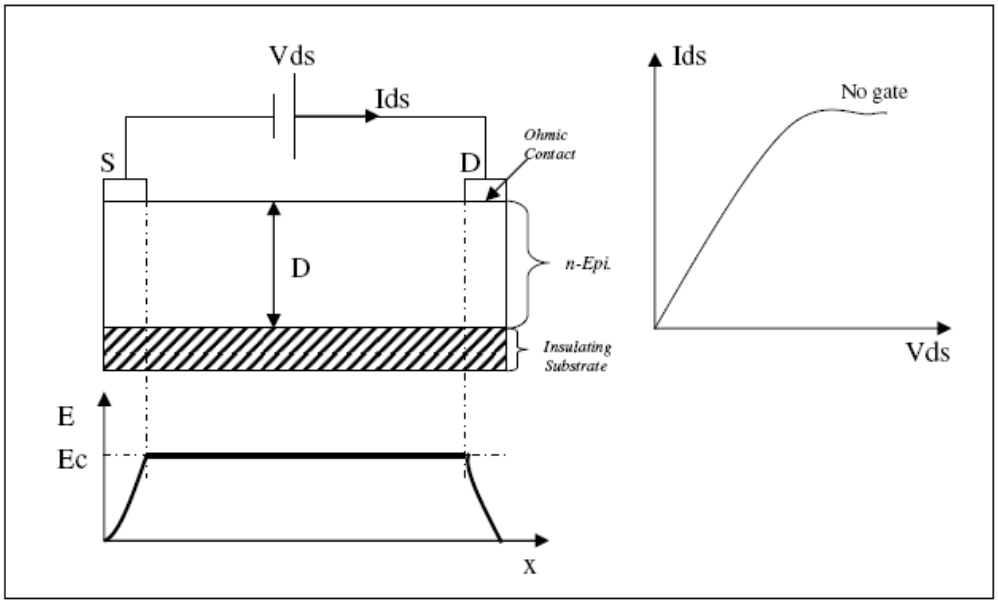

Figure**1**. 1: I-V characteristics of an n-type 4H-SiC layer with two ohmic contacts and without gate [4]

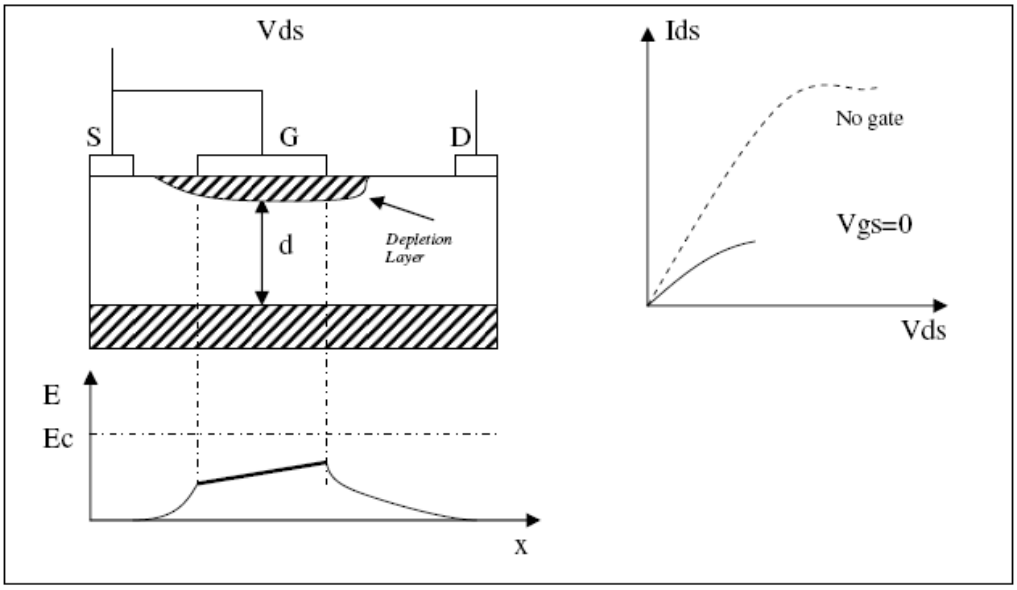

Figure 1.3 I-V characteristics of an n-type 4H-SiC layer with two ohmic contacts and a metal contact as gate [4].

In Figure 1.3, a metal-to-semiconductor contact, called the gate, has been added between source and drain. This contact creates a layer in the semiconductor that is completely depleted of free-carrier electrons. This depletion layer acts like an insulating region and constricts the channel

available for current flow in the n layer. The width of the depletion region depends on the voltage applied between the semiconductor and the gate.

In Figure 1.4, the gate is shorted to the source and a small drain voltage is applied. Under these conditions, the depletion layer has a finite width and the conductive channel beneath has a smaller cross section d than in Figure1.3. Consequently, the resistance between source and drain is larger.

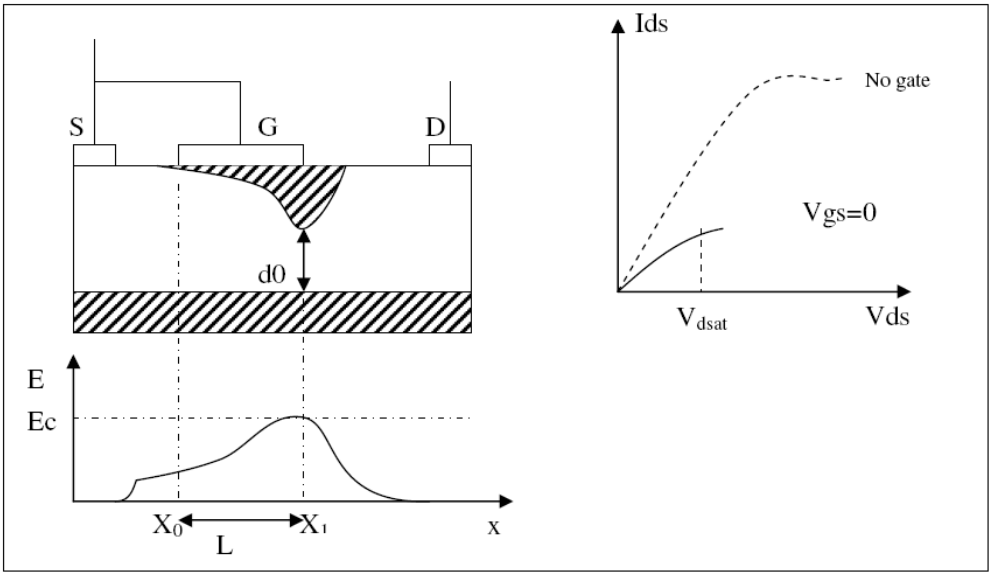

Figure 1.4: V_{ds}–I_{ds} Representation with respect to V_{gs} with shorted source and gate

If the drain voltage is increased beyond V_{Dsat}, the depletion region widens toward the drain. The pointx_1, where the electrons reach the limiting velocity, moves slightly toward the source in Figure 1.5. As x_1 moves closer to the source, the voltage at x_1 decreases. Therefore, the conductive cross section d_1 widens and more current is injected into the velocity-limited region. This results in a positive slope of the I_{Ds} curve and a finite drain-to-source resistance beyond current saturation. The effect is particularly prominent in microwave MESFETs with short gate

lengths. going on from x_1 toward the drain, the channel potential increases, the depletion layer widens, and the channel cross section *d* becomes narrower than d_1 [4-5].

Since the electron velocity is saturated, the change in channel width must be compensated for by a change in carrier concentration to maintain constant current. An electron accumulation layer forms between x_1 and x_2, where d is smaller than d_1. At x_2 the channel cross section is again d_1 and the negative space charge changes to a positive space charge to preserve constant current.

The positive space charge is caused by partial electron depletion. The electron velocity remains saturated between x_2 and x_3 due to the field added by the negative space charge. In short, the drain voltage applied in excess of V_{Dsat} forms a dipole layer in a channel that extends beyond the drain end of the gate [4].

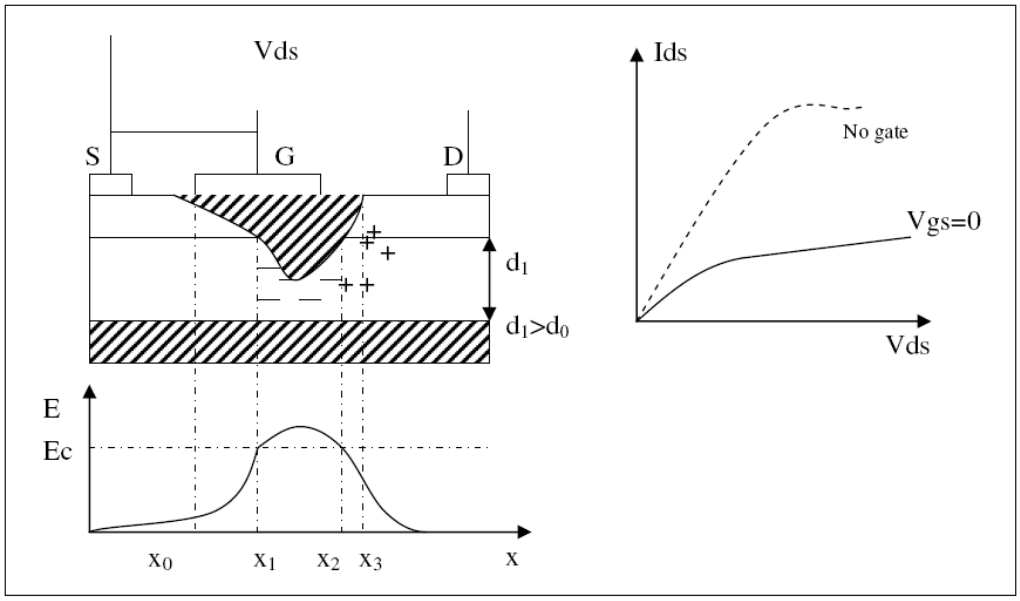

Figure 1.5 $\boldsymbol{V_{ds} - I_{ds}}$ Representation with respect to $\boldsymbol{V_{gs}}$ with more widening of depletion region [5]

When a negative voltage is applied to the gate (Figure 1.6), the gate-to channel junction is reverse biased, and the depletion region grows wider. For small values of V_{ds}, the channel will

act as a linear resistor, but its resistance will be larger due to a narrower cross section available for current flow. As $V_{ds}$is increased, the critical field is reached at a lower drain current than in the $V_{gs} = 0$ case, due to the larger channel resistance. For a further increase in V_{ds}, the current remains saturated. In essence, the MESFET consists of a semiconducting channel whose thickness can be varied by widening the depletion region under the metal-to-semiconductor junction. The depletion region widening is the effect of a field or voltage applied between gate and channel of the transistor.

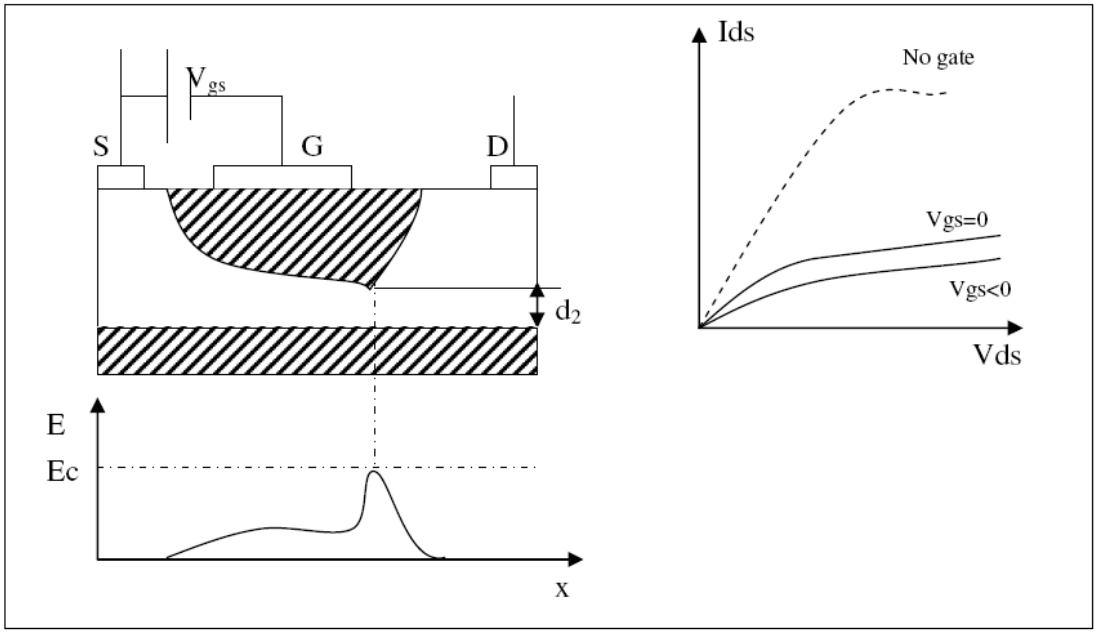

Figure **1.6**: $\boldsymbol{V_{ds} - I_{ds}}$ Representation with respect to negative gate to source voltage

1.2.2 I-V Characteristics of MESFET

As mentioned above the source and drain terminals are ohmic contacts and gates are schottky contact. Most MESFET devices are Depletion Mode Devices i.e., the device with n-type conductive channel at $V_g = 0\,V$. This means that in the presence of applied reverse gate bias, current can flow between the source and drain contacts. Enhancement Mode Devices do not

conduct current between the drain and source unless forward gate bias is applied (no conductive channel at $V_g = 0\ V$). For depletion mode devices, when low bias voltages are applied between the source and the drain contacts, a current flows through the channel. The current is linearly related to the voltage across the terminals. For higher drain-source voltage levels, the electrons in the semiconductor material will attain their maximum carrier.

The gate contact in a MESFET device is a Schottky barrier. The energy band bending produced by making Schottky barrier contact with the semiconductor creates a layer below the gate that is completely depleted of free charge carriers. As no free carriers exist in this depletion layer, no current can flow through it. The available channel region for current flow is reduced due to existence of this depletion layer. As reverse bias is applied to the gate, the depletion layer penetrates deeper into the active channel. These further reductions in channel region result in further reduction of current. Then the gate voltage acts as a means for limiting the maximum amount of source-drain current that can flow. When enough reverse bias is applied, the depletion region will extend across the entire active channel and allow essentially no current to flow. That gate-source potential is termed as the "Pinch-off voltage".

1.3. Trapping Effect

It is fact that trapping effects limit the output power performance of microwave field-effect transistors (FETs). This is mostly true for the wide band gap devices. There are energy level in the band gap which are neither donor nor acceptor such centre captures one or another type of carrier release by thermal emission such centers are called traps and there effects are such that the carrier lifetime, hence conductivity are reduced.

1.3.1 Trapping Effect of 4H-SiC MESFET

We know that, 4H-SiC exhibits a high breakdown field and a high saturated electron velocity. Silicon carbide also offers a high thermal conductivity, making it a natural choice for high-power electronics. However SiC microwave devices are at a distinct disadvantage for high-frequency applications due to traps. With the realization of large-area semi-insulating (SI) 4H-SiC substrate material, larger FET structures could be fabricated for higher output powers without suffering the large parasitic capacitive losses of previous devices grown on n^+ substrates. As a result of this effect, the RF power output of these devices was observed to be inferior to that of devices grown on n^+ substrates. In addition, with increasing negative gate bias, the effect became more severe. It was, thus, concluded that the traps responsible for this effect were probably associated with the SI substrate or the substrate/p-buffer layer interface [6].

1.3.2 Major impurities for deep level Traps of 4H-SiC MESFET [7]

Nitrogen. Specially undoped SiC layers have n-type conductivity. In addition, nitrogen has a fairly high solubility in SiC and the lowest ionization energy of all the impurity donor levels. By implanting N ions it is also possible to obtain thin, heavily doped layers of SiC for forming ohmic contacts [7].

Aluminum. The p-type silicon carbide is customarily obtained using Al, which forms the shallowest acceptor levels in the lower half of the band gap and has the highest solubility.

Boron. Boron forms acceptor levels and can be used to make p-n junctions. It has a high solubility, $(10^{20}\ cm^{-3})$, and is one of the most rapidly diffusing impurities in 4H-SiC.

Other impurities centers are Gallium, Indium, Vanadium, Manganese, L-centre, I-centre, D-centre, Z $1/2$, RD $1/2$, EH $6/7$ etc. [7-8].

1.4 Literature review

It is known fact that trapping effects limit the output power performance of 4H-Silicon carbide MESFET. This is mainly true for the wide band gap devices. In 2001, Steven C. Binari *et al*. [6] review the various trapping phenomena observed in SiC-MESFETs that contribute to compromised power performance. For these material systems, trapping effects associated with both the surface and with the layers underlying the active channel have been identified. The measurement techniques and steps taken to identify these traps and minimize their effects.

In 2003 A.P. Zhang *et al*. [9] has compared the performances of silicon carbide (SiC) metal semiconductor field-effect transistors (MESFETs) fabricated on conventional Vanadium-doped semi-insulating substrates and new V-free semi-insulating substrates. They confirmed that under various DC and RF condition, 4H-SiC MESFETs fabricated on new V-free semi-insulating substrates showed better device performance and stability.

In the same year Nabil Sghaier *et al*. [10] demonstrates about the Study of Trapping Phenomenon in 4H–SiC MESFETs which mainly point about the substrate purity. They investigated that 4H–SiC MESFETs. Structures realized on two types of S.I substrates. The first kind is vanadium doped substrates grown by the classical Physical Vapor Transport (PVT) sublimation technique. The second kind are extremely low vanadium content semi-insulating substrates grown by the high temperature (HTCVD) technique.

In 2004, Sankha S. Mukherjee *et al*. [11] described An analytical model of SiC MESFET incorporating trapping and thermal effects. Temperature dependencies of carrier transport parameters and trapping effects was taken into account. For calculating the observed current slump in the I–V characteristics, they had taken both surface and substrate traps into the model.

They also described about detrapping process by increasing drain bias which is accelerated by increased thermal effects.

In 2006, Shabna Asmi *et al*. [12] presented a small signal non-quasi-static model for SiC MESFET. The model incorporates the effect of traps and self-heating on high frequency operation. They had included both the dc and ac characteristics of the MESFET. They concluded that decrease of the trap density from $10^{16}\ cm^{-3}$ to $10^{14}\ cm^{-3}$ increases the cutoff frequency by about 40%.

In the same year, Andrei V. Los [13] presented an experimental model of dc and small-signal ac drain-source characteristics of 4H silicon carbide metal-semiconductor field-effect transistors fabricated on vanadium-compensated semi-insulating substrates, with and without a low-doped p-type buffer layer. He concluded that dc and transient output characteristics are approx. similar in both types of the MESFETs with a significant drain current degradation and hysteresis observed experimentally at large gate voltages.

In 2007, W. C. Mitchel *et al*. [14] has been made study of deep levels in high purity semi-insulating 4H-SiC using temperature dependent Hall effect (TDH), thermal and optical admittance spectroscopy, and secondary ion mass spectrometry (SIMS). They had given view of deep level trap about activation energy, acceptor or donor type etc. they also suggested about compensation mechanism for making semi-insulating substrate.

In 2010, Hans Hjelmgren *et al*. [15] have been simulated transient characteristics of a SiC metal–semiconductor field-effect transistor by taking Self-heating, gate tunneling, substrate, and surface traps into account. They had proposed that to simulate any gate lag in a SiC MESFET with surface acceptors situated close to the conduction band, there has to be a trap filling current during pinch off.

1.5 Scope of this thesis

4H-SiC MESFET is widely used in microwave circuits, wireless communication, high power, high frequency operation due to its superior properties like wide band gap, high breakdown field, high saturated electron velocity etc. But in this work, several problems arise due to trapping effect, self heating effect, channel length modulation, source and drain resistance etc.

After doing literature survey, many important observations comes in front of me that regarding the analytical modeling of 4H-SiC MESFET some researchers has done analytical modeling of 4H-SiC MESFET by taking single trap level into account. Most of the earlier studies are concentrated on the modeling without taking effect of field dependent mobility. But in this work we considered this one which may help in optimization of the device performance under high electric field velocity saturation.

In this thesis, there is consideration of three different trap concentrations in 4H-SiC substrate with channel length modulation in saturation region which may useful for understanding the physical characteristics of the device in the saturation region with more accuracy.

We have done simulation of I-V characteristics by considering self heating effects and also described about the changed parameter due to change in temperature. This work may help the researchers in designing microwave circuits at high temperature operation.

Chapter 2

I-V characteristics of 4H-SiC MESFET without Trap Effects

In order to investigate the effects of traps on I-V characteristics, a set of DC I-V characteristics without trap effects have been performed.

A schematic diagram of MESFET is shown in fig. The MESFET consist of a conductive channel provided with two ohmic contacts, one as the source and other as drain. When a positive voltage V_D is applied to the drain with respect to source, electron flow from source to drain. Hence source acts as the origin of the carriers and drain acts as the sink. The third one, the gate forms a rectifying junction with the channel. The device is basically a voltage controlled resistor, and its resistance can be varied by width of depletion layer extending into channel region.

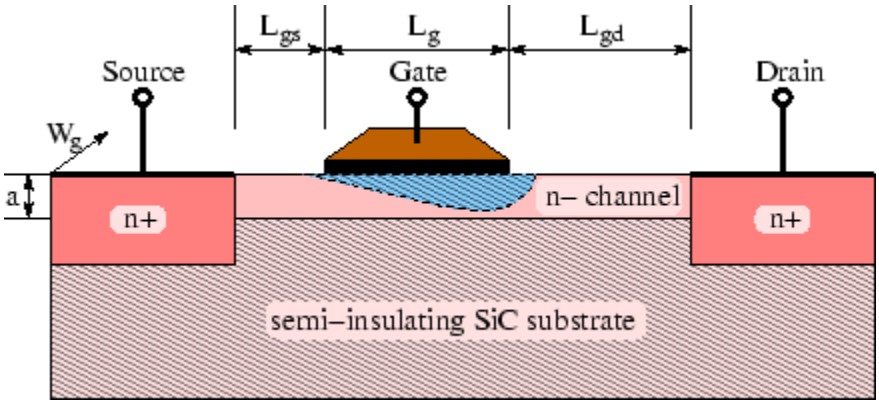

Figure2.1 : Cross section of a MESFET in 4H-SiC substrate. With channel length L, channel width z, channel depth a.

The basic current voltage characteristic of MESFET is shown in fig. where the drain current is plotted against the drain voltage for various gate voltages in positive side. And in negative side drain current is plotted against the gate voltage. This I-V characteristic is divided into two

regions: the linear region where the drain voltage is small and I_D is proportional to V_D and second one is saturation region where the current remains mainly constant and is independent of V_D.

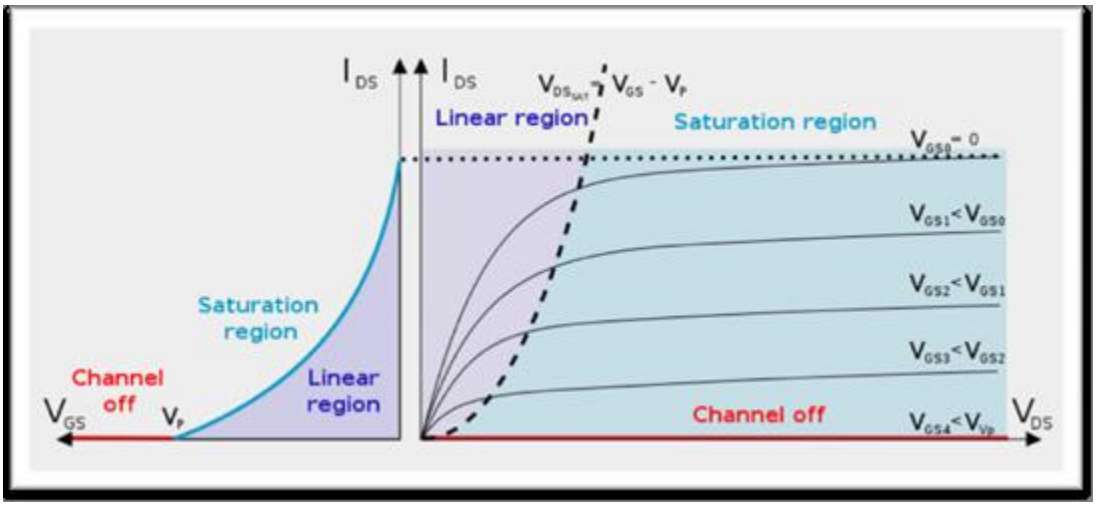

Figure 2.2 Basic I-V characteristics of MESFET which include linear region and saturation region

2.1 Theoretical Model of I-V characteristics

The current at point x in the channel in the linear region is given by [4].

$$\boldsymbol{I_D = I_p\left\{3\frac{V_D}{V_p} - 2\left[\frac{\left(V_D + V_g + V_{bi}\right)^{1.5} - \left(V_g + V_{bi}\right)^{1.5}}{V_p{}^{1.5}}\right]\right\}} \qquad (\mathbf{2.1})$$

This is for linear region where $V_D < V_{Dsat}$

where I_p is the pinch-off current,

$$I_p = \frac{z\mu q^2 N_d^2 a^3}{6\varepsilon_s L} \qquad (2.2)$$

V_{bi} is the built in potential between the p-n junctions and is given by:

$$V_{bi} = \left(\frac{KT}{q}\right) l\, n \left(\frac{N_d}{n_i}\right) \tag{2.3}$$

V_p is the pinch off voltage:

$$V_p = \frac{\mathrm{qN_d a^2}}{2\varepsilon_s} \tag{2.4}$$

and n_i is the intrinsic carrier concentration is given by [3]

$$n_i = (N_c . N_v)^{0.5} . e^{\left(\frac{-E_g}{2KT}\right)} \tag{2.5}$$

In which μ is the mobility which is assumed to be field independent, $\mathrm{N_d}$ is the channel doping concentration, ε_s is the permittivity of 4H-SiC , N_c and N_v are the density of state in conduction band and valence band resp[3]. E_g is the energy band gap, K is Boltzmann constant and T is Temperature in Kelvin.

For a given $\mathrm{V_g}$, the maximum current I_{Dsat} occurs at the point where the channel is pinched off. The current is obtained as

$$I_{Dsat} = \mathrm{I_p}\left[1 - 3\left(\frac{\mathrm{V_g + V_{bi}}}{\mathrm{V_p}}\right) + 2\left(\frac{\mathrm{V_g + V_{bi}}}{\mathrm{V_p}}\right)^{1.5}\right] \tag{2.6}$$

This is for saturation region where $\mathrm{V_D} < V_{Dsat}$

Where saturation volage is given by:

$$V_{dsat} = \frac{\left(\mathrm{V_g - V_t}\right).\mathrm{F_s}.\mathrm{L}}{\mathrm{V_g - V_t + F_s}.\mathrm{L}} \tag{2.7}$$

$\mathrm{V_t}$ is threshold voltage:

$$V_t = \mathrm{V_{bi} - V_p} \tag{2.8}$$

For drain voltage beyond V_{dsat}, the drain current is assumed to remain same as the saturation current [4].

2.2 Experimental Evaluation and Simulation Result

Accurate theoretical models of 4H-SiC material properties are a precondition for device simulation. available material data were utilized to derive physical models by adjusting model parameters to obtain the closest possible agreement with experimental data. It is known fact that as the drain voltage increases the depletion region at the edge of the gate extends toward the drain side. This extension becomes significant in 4H-SiC MESFETs which operate at high drain voltages.

The details of the 4H–SiC material parameter and device dimension used in the simulations are shown in table [16].

Table 2.1: Parameters and dimensions used in simulation of 4H-SiC MESFET

$z = 332\ \mu m$	$a = 0.26\ \mu m$
$\mu = 560\ cm^2/vs$	$\varepsilon s = 9.7x8.85x10 - 14\ F/cm$
$q = 1.6x10 - 19\ \ c$	$Eg = 3.26\ eV$
$N_d = 1.7x1023\ m^{-3}$	$N_c = 1.23x1025\ m^{-3}$
$L = 0.7\ \mu m$	$N_v = 4.58x1024\ m^{-3}$

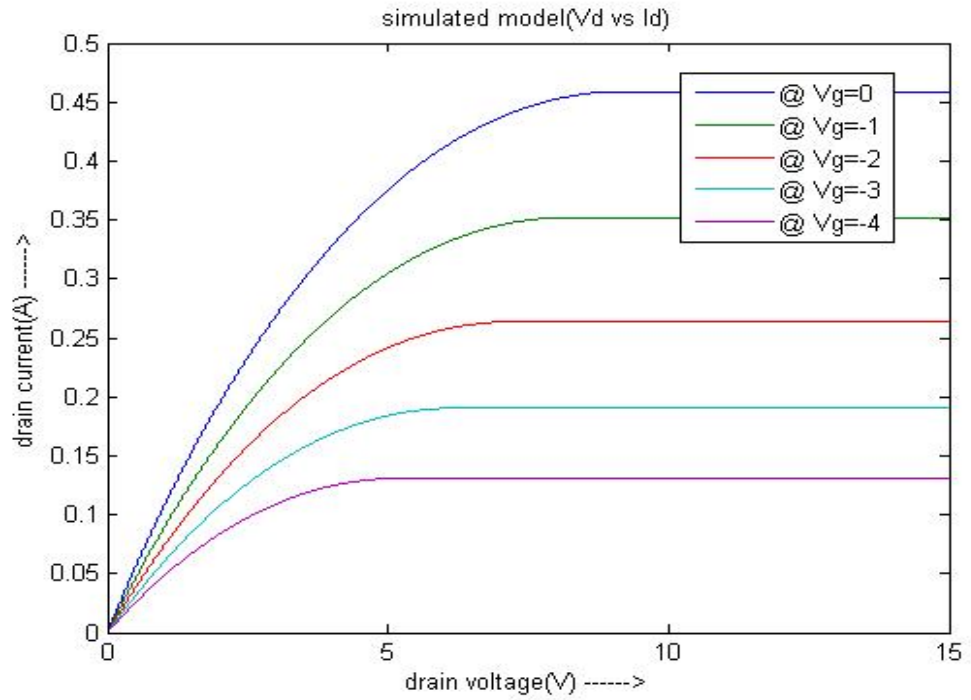

Figure 2.3: Simulated I-V characteristics of 4H–SiC MESFET at different gate voltage V_g.

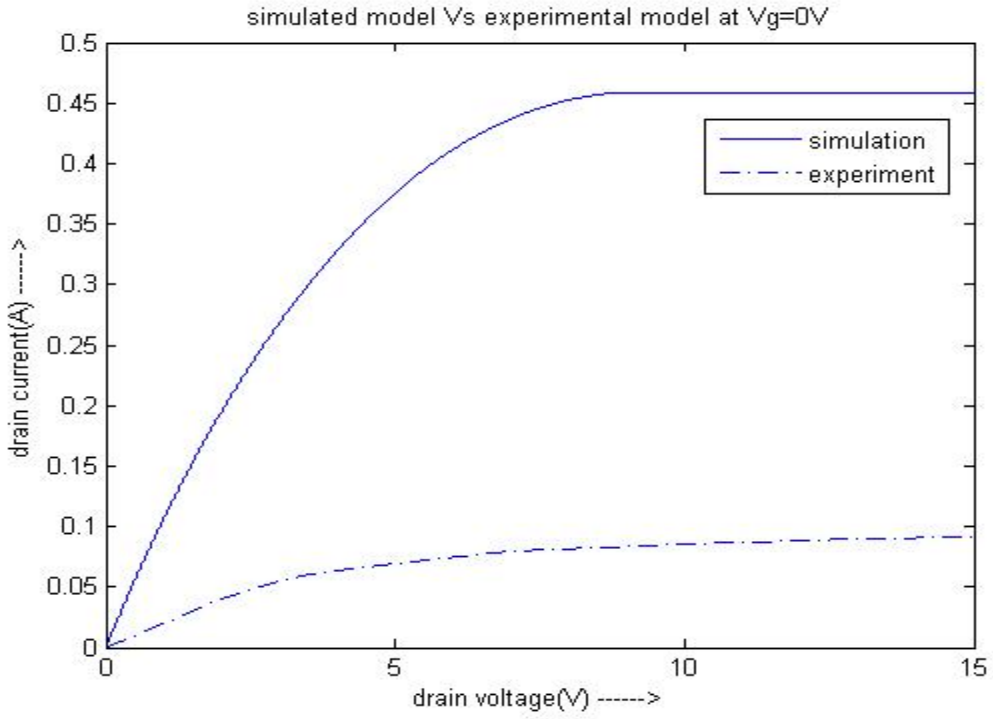

Figure 2.4: Comparison of experimental [16] and simulated results of I-V characteristics of 4H–SiC MESFET

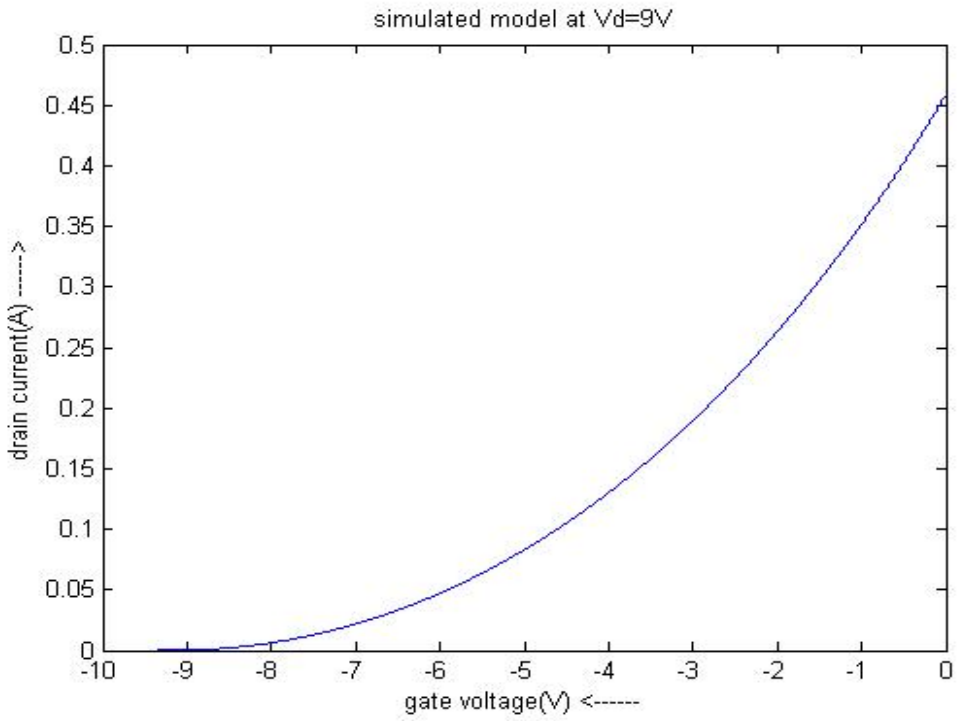

Figure 2.5: I_D-V_g characteristics of 4H-SiC MESFET at $V_D = 9V$

2.3 Summary

In this chapter, just a theoretical model has been presented in both linear and saturation region without taking any trap parameter. In first simulation, model of I_D Vs V_D is presented at different V_g which fully satisfied our theoretical result in both linear and saturation region. In second simulation we compared our result with experimental result and we can seen that at $V_g = 0$ V, measured SiC MESFET yielded a drain current of 450 mA at a drain voltage of 15 V. But experimental result produces much less drain current of around 100 mA at same drain voltage which is due to trap effect. So my main aim is to make closer to experimental result by introducing single trap level, multiple deep level trap, self heating effect etc. for making good accuracy and verify the model which is done in further chapter.

Chapter 3

I-V Characteristics of 4H-SiC MESFET with single Trap level

3.1 Introduction

In this chapter, the main work highlighted on electron traps in semi-insulating (S.I) 4H-SiC Substrate. We know that trapping effects can limit the output power performance of microwave field-effect transistors (FETs). Due to Trap of electron in substrate from channel, substrate become not behaves as a semi –insulating and it reduces the drain current in channel. Both experimental and theoretical work has been done to determine the parameters of the trap.

4H-SiC device's drain current are significantly limited by a relatively high density of defects, acting as carrier traps and thus worsening device performance and efficiency. Therefore, it is necessary to investigate such traps in various detectors and develop methods to examine and determine their parameters.

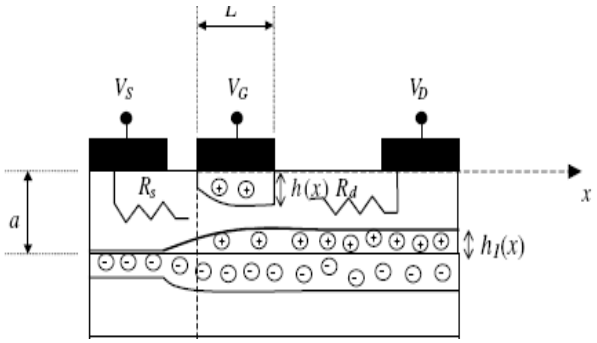

Figure 3.1: 4H-SiC MESFET substrate showing the depletion regions at the gate–channel and channel–substrate interfaces and the source and drain resistances due to trap of electron.

In Fig. 3.1, the depletion region below the schottky gate and the other depletion region is formed at the channel-substrate interface due to the deep level traps in the SI substrate. The widths of these depletion regions are strongly dependent on the substrate properties as well as on

the gate voltage which in turn effects current flowing through the channel. Thus, substrate induced effects are crucial in determining I-V characteristics of the device.

3.2 Model of I–V characteristics including trap effect

Considering velocity saturation and the depletion layers formed in the channel at the gate due to the gate bias and at the channel/substrate interface due to the trapped carriers. So, in our proposed model, we can see the reducing value of current I_D in channel by considering doping concentration in substrate, trap concentration, positive charge concentration in depletion region etc.

The concentration of negative charge in the substrate side of the CS junction [17] is

$$N_{sub} = N_{trap}(non - eql) - N_{trap}(eql) \tag{3.1}$$

$$= \left\{N_{trap}\left(\frac{e_p}{e_p+e_n}\right)\right\} - \left\{N_{trap}\left\{1 + \frac{1}{2}\exp\left[\frac{(E_t-E_{fs})}{KT}\right]\right\}^{-1}\right\} \tag{3.2}$$

Where $N_{trap}(eql)$ is the density of occupied traps in the bulk substrate under thermal equilibrium condition.

Where E_{fs} is the Fermi energy level in the substrate bulk which is calculated graphically [18], E_t is energy of the trap level ($= 0.65$ eV from conduction band) , N_{trap} is the Trap Concentration($\approx 1x10^{22}$ m^{-3}) [16], e_p and e_n are the emission rates of holes and electrons from Trap levels respectively which is given by following expression[20].

$$e_{p/n} = \sigma_{p/n}.v_{p/n}.N_{v/c}exp\left(\frac{-\Delta E}{KT}\right) \tag{3.3}$$

And $$v_{p/n} = \sqrt{\frac{3KT}{m^*_{p/n}}} \tag{3.4}$$

Where p and n denote holes and electrons, e is the emission rate, σ is the capture cross-section, v is the thermal velocity, $N_{v/c}$ is the effective density of states in the valence/conduction band , ΔE is the energy separation between the trap level and the valence/conduction band and $m^*_{p/n}$ effective mass of hole / electron .

Assuming that N_d, N_{SA} and N_{SD} are fully ionized in the active layer. The total positive charge concentration in the depletion regions [17] becomes

$$N_{dep} = N_d + N^D_{trap} - (N_{SA} - N_{SD}) \tag{3.5}$$

Where N_{SA} and N_{SD} ionized shallow acceptor and ionized shallow donor concentrations in the bulk substrate under equilibrium condition respectively with $N_{SA} - N_{SD}$ ≈5x10^{20} [14].

And N^D_{trap} is the concentration of ionized trap states in depletion regions of 4H-SiC MESFET Neglecting the free carrier concentrations in the depletion regions ($n = p = 0$), the concentration of ionized trap states in these depletion regions may be given by

$$N^D_{trap} = N_{trap}\left(\frac{\mathrm{e_n}}{\mathrm{e_p} + \mathrm{e_n}}\right) \tag{3.6}$$

So the analytical expression for the I-V characteristics in linear region including trap parameter [17]

$$I_D = I_p\left\{3\frac{V_D}{V_p} - 2\left[\left(\frac{V_D+V_g+V_{bi}}{V_p}\right)^{1.5} - \left(\frac{V_g+V_{bi}}{V_p}\right)\right] - 2\left(\frac{N_{sub}}{N_{dep}+N_{sub}}\right)\left(\left(\frac{V_D+V_{bi}}{V_p}\right)^{1.5} - \left(\frac{V_{bi}}{V_p}\right)^{1.5}\right)\right\} \tag{3.7}$$

Where Ip is pinch-off current which is constant

$$I_p = \frac{\mathrm{z\mu q^2(N_d} - N_{sub})(N_{dep})\mathrm{a^3}}{6\varepsilon_s.\,\mathrm{L}} \tag{3.8}$$

Equation (3.7) is harshly valid in the linear region,

When electric field in the channel reaches saturation electric field (E_s) at $V_D = V_{Dsat}$

$$\text{Then} \quad I_{Dsat} = I_D(V_D = V_{Dsat}) \tag{3.9}$$

3.3 Model for calculating Fermi level

The calculation of the position of the Fermi level is of basic importance in solid state electronics for the characterization of the transport properties of semiconductors and devices. Following is an graphical method developed [18] for determining energy Fermi level from the neutrality condition.

$$n + N_{SA}^{-} + N_{Trap}^{-} = p + N_{SD}^{+} \tag{3.10}$$

In large gap semiconductors the Fermi level is within the band gap several kT units away from the band edges. So the expression of free electron concentration, n is given by

$$n = N_c . \frac{exp(E_g - E_{fs})}{KT} \tag{3.11}$$

The ionized shallow acceptor concentration as the function of energy can be determined by:

$$N_{SA}^{-} = N_{SA} \left(\frac{1}{1 + \frac{1}{g} \frac{exp(E_A - E_{fs})}{KT}} \right) \tag{3.12}$$

The ionized negative trap concentration in the substrate is given by

$$N_{Trap}^{-} = N_{trap} \left(\frac{1}{1 + \frac{1}{g} \frac{exp(E_T - E_{fs})}{KT}} \right) \tag{3.13}$$

The hole concentration, p, is given by the equivalent expression

$$p = N_v . \frac{exp(-E_{fs})}{KT} \tag{3.14}$$

The ionized shallow acceptor concentration is given by the following expression

$$N_{SD}^{-} = N_{SD} \left(1 - \left(\frac{1}{1 + \frac{1}{g} exp(E_D - E_{fs})} \right) \right) \tag{3.15}$$

The Fermi level can now be determined by plotting the terms in equation (3.10) as a function of energy, E, using the above given expressions in equation. (3.11) to (3.15).

3.4 Simulation Result

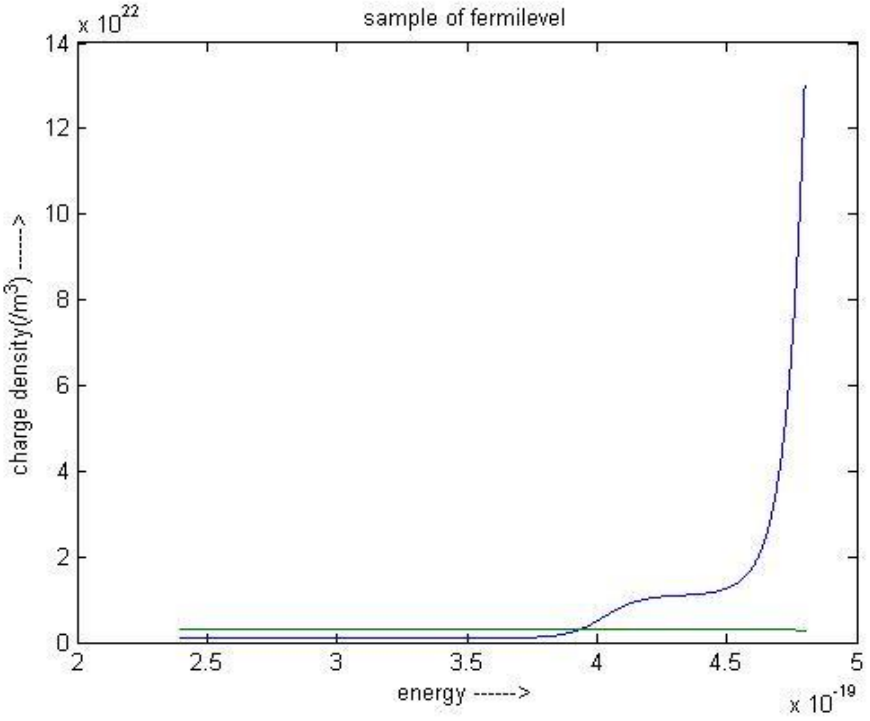

Figure 3.2: Simulated graphical curves for position of Fermi level of S-I 4H-SiC MESFET

$E_{fs} = 3.9/1.6 = 2.43\ eV$ from valence band

So the value of energy Fermi level from conduction band $= 3.2 - 2.43 = 0.77\ eV$

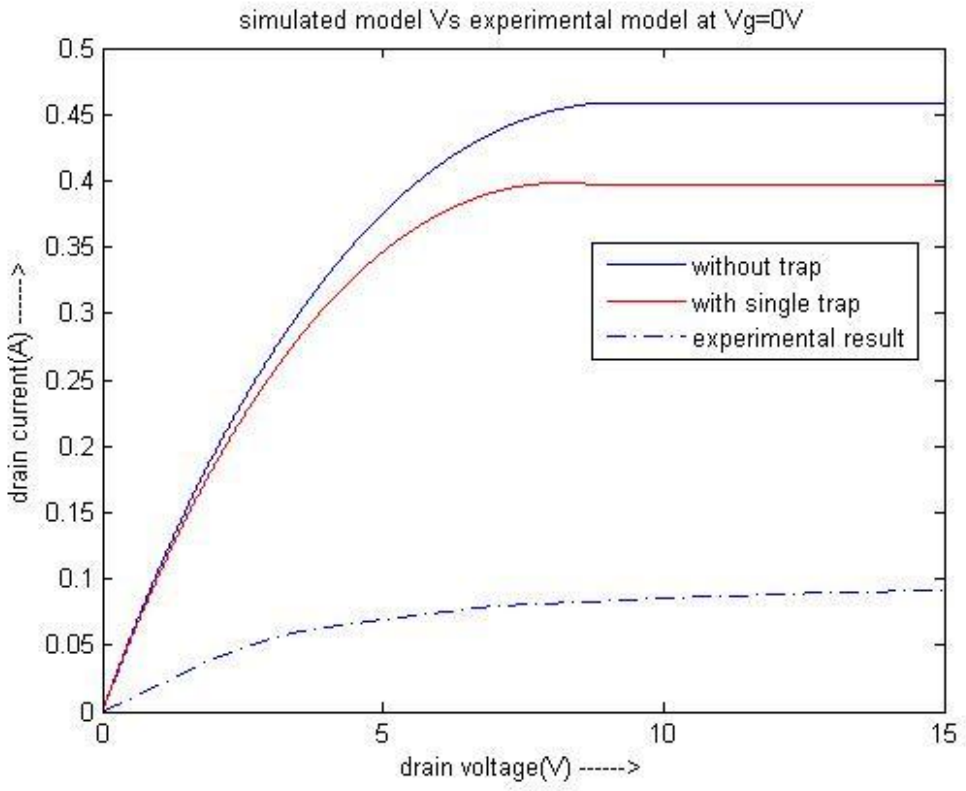

Figure 3.3: simulation of I-V characteristics of 4H-SiC MESFET with single trap level

3.5 Summary

Now we can see the reducing value of drain current by including single trap parameter which make little close to experimental model. But in practically there is multi deep level trap. Further we can see that drain current is also affected by field dependent mobility, self heating effect, source and drain resistance.

Chapter 4

An Improved I-V Model of 4H-SiC MESFETs with Multiple Deep Level Traps (DLT) and self heating effect

4.1 Introduction

semi-insulating nature of the substrate is modeled by considering three dominant intrinsic deep acceptor-like traps responsible for carrier compensation in HPSI 4H-SiC substrates for the first time. To further improve the accuracy, field–dependent mobility of electrons in the linear region and channel-length modulation in saturation region are considered in deriving the static I-V characteristics in addition to the substrate effects. The temperature dependence of carrier trapping and detrapping into/from the multiple deep levels and the corresponding I-V variations is analytically studied. Moreover, this model includes source and drain series resistances which are significant in 4H-SiC due to less low-field mobility of electrons compared to GaAs.

4.2 An analytical I-V model with multiple deep level traps

The mostly three deep level traps observed in 4H-SiC substrate $Z_{1/2}$[14], $RD_{1/2}$, $EH_{6/7}$ [8]. Most researchers report that the intrinsic deep levels observed by DLTS in the upper half of the band gap are acceptor like. These trap have been listed separately because of the differences in capture cross section coefficient which is shown in table 4.1.

Table 4.1: Deep levels by DLTS reported in the literature in the upper half of the band gap of 4H-SiC with location of trap level from conduction band

Name of Trap	Trap location(eV)	Trap conc.(N_t) /cm^3	Trap c/s of electron σ_n (cm^2)	Trap c/s of hole σ_p (cm^2)
$Z_{1/2}$	0.67	$3.8x10^{15}$	$2x10^{-14}$	$3.5x10^{-14}$
$RD_{1/2}$	0.93	$2x10^{15}$	$5x10^{-15}$	$1x10^{-17}$
$EH_{6/7}$	1.65	$3x10^{15}$	$2.4x10^{-13}$	$1x10^{-15}$

By using the above Trap parameter we can calculate the emission rate of a hole/electron trap by using the expression of emission rates at temp $300\ k$ which is shown in below table 4.2.

$$e_{p/n} = \sigma_{p/n}.v_{p/n}.N_{v/c}exp\left(\frac{-\Delta E}{KT}\right) \tag{4.1}$$

Table 4.2: emission rates of electron and holes of different trap

Name of Trap	Emission rates of electron $e_{n\,(/cm^3sec)}$	Emission rates of hole $e_{p\,(/cm^3sec)}$
$Z_{1/2}$	0.2516	0.08
$RD_{1/2}$	$2.72x10^{-6}$	$9.9x10^{-10}$
$EH_{6/7}$	$1.07x10^{-16}$	$8.15x10^{-20}$

The net concentration of negative charge, at equilibrium, on the substrate side of the substrate-channel region interface N_{sub} [19] depends on the occupancy of the deep traps in the bulk according to the following relationship:

$$N_{sub} = N_{trap1}\left(\frac{e_{p1}}{e_{p1}+e_{n1}}\right) - \left(\frac{1}{1+exp\left(\frac{E_{t1}-E_{fs}}{KT}\right)}\right) + N_{trap2}\left(\frac{e_{p2}}{e_{p2}+e_{n2}}\right) - \left(\frac{1}{1+exp\left(\frac{E_{t2}-E_{fs}}{KT}\right)}\right) + N_{trap3}\left(\frac{e_{p3}}{e_{p3}+e_{n3}}\right) - \left(\frac{1}{1+exp\left(\frac{E_{t3}-E_{fs}}{KT}\right)}\right) \tag{4.2}$$

Therefore the analytical expression for the I-V characteristics in linear region including multi deep level trap as defined for single level trap.

$$I_D = I_p \left\{ 3\frac{V_D}{V_p} - 2\left[\left(\frac{V_D + V_g + V_{bi}}{V_p} \right)^{1.5} - \left(\frac{V_g + V_{bi}}{V_p} \right) \right] - 2\left(\frac{N_{sub}}{N_d + N_{sub}} \right) \left(\left(\frac{V_D + V_{bi}}{V_p} \right)^{1.5} - \left(\frac{V_{bi}}{V_p} \right)^{1.5} \right) \right\} \quad (4.3)$$

And for saturation region

$$I_{Dsat} = I_D(\mathrm{V_D} = V_{Dsat}) \quad (4.4)$$

4.3 Effects of field dependent mobility on I-V characteristics

At low electric field the velocity increases linearly with the field and the slope corresponds to a constant mobility ($\mu = dv/dE$). But for high field velocity saturation, drift velocity not become saturation velocity, it depends upon electric field which is shown by analytical expression for the drift velocity of 4H-SiC [4].

$$v = \frac{\mu E_x}{1 + \mu \frac{E_x}{v_s}} \quad (4.5)$$

Where μ is the low field mobility, v_s is the saturation velocity and $E_x = {}^{dV}/_{dx}$ is the longitudinal field in the channel.

By using sze's model [4] we get new I-V model in which drain current is reduced by the factor of $1 + \frac{\mu V_D}{v_s L}$ due to field dependent mobility.

4.3.1 Simulation Result

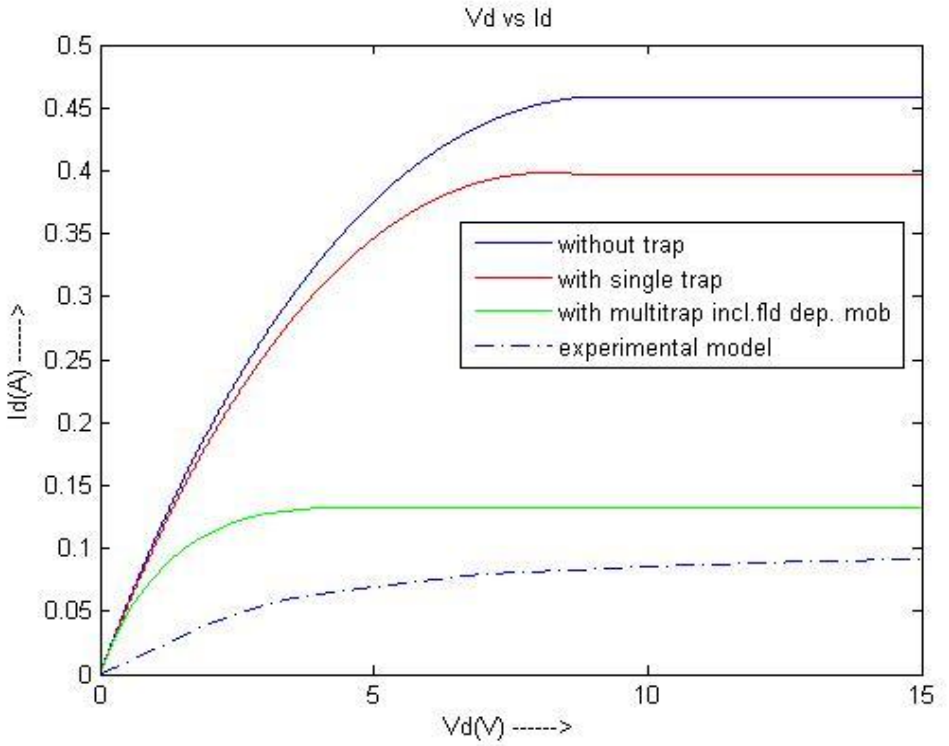

Figure 4.1: Simulated model of I-V characteristics of multi deep level trap including field dependent mobility (green line) comprised with experimental model (dashed line)

4.3.2 Summary

In this simulated model, as we include three different trap ($Z_{1/2}$, $RD_{1/2}$, $EH_{6/7}$) with field dependent mobility, the value of drain current reduced to around 140 mA from 400 mA which is caused by single trap level. Now we can see that it comes more close to experimental model.

4.4 Effect of Source and Drain Resistance on I-V characteristics of 4H-SiC MESFET

source and drain resistances strongly influence the MESFET's performance . The increased influence of resistances R_s and R_D is due to the source-to-gate length L_{GS} and the drain-to-gate length L_{GD} not decreasing proportionally as the gate length is decreased.

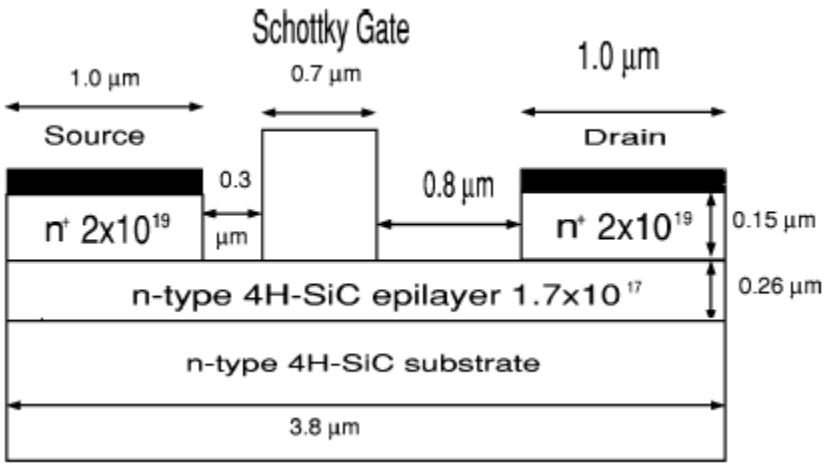

Figure 4.2: Structure of the simulated 4H-SiC MESFET. The gate width is 332 mm. The gate length is 0.7 mm, and the source-gate and gate-drain spacing are 0.3 and 0.8 mm, respectively [16].

We know that

$$R_S = \rho \frac{L_{GS}}{A} \tag{4.6}$$

$$R_D = \rho \frac{L_{GD}}{A} \tag{4.7}$$

Where ρ is the resistivity

$$\rho = \frac{1}{q.\mu.N_d} \tag{4.8}$$

So by using parameter value from Table 2.1, we can calculate the value of Rs and R_d

So modified value of gate and drain voltage

$$V_{gs} = V_g - I_D.R_S \tag{4.9}$$

$$V_{DS} = V_D - I_D.(R_S + R_D) \tag{4.10}$$

By using this modified gate and drain voltage in place of original gate and drain voltage, we can calculate the reduced drain current by source and drain resistance.

4.5 Dependency of saturation region on effective length

In above equation of drain current, we assumed that the channel length is constant. When MESFET is biased in saturation region depletion regions at drain end of gate extends laterally into the channel reducing the effective channel length. In a physical model, channel length modulation is the shortening of length of the channel region with increase in drain voltage for large drain voltage. The effective channel length of MESFET in saturation region [17] is

$$L_{eff} = L - L_s \tag{4.11}$$

$$L_s = 2.06\, K_d \left(\frac{\varepsilon_s (V_{Ds} - V_{sat})}{q\sqrt{n_{cr} N_d}} \right)^{1/2} \tag{4.12}$$

L_s is the length of velocity saturation region below gate, K_d is a domain parameter [20] and n_{cr} is the characteristic doping density of 4H-SiC [20].

$$n_{cr} = \frac{\varepsilon_o \varepsilon_r \mu E_{ch}^2}{qD} \tag{4.13}$$

Where E_{ch} is the characteristics electric field and D is the electron diffusion coefficient (5.3 cm^2/sec).

Analytical expression for pinch-off current in saturation region is,

$$I_p = \frac{z\mu q^2 (N_d - N_{sub})(N_{dep}) a^3}{6\varepsilon_s . L_{eff}} \tag{4.14}$$

According to this, drain current changes in saturation region due to changed in effective length.

4.5.1 Simulation Result

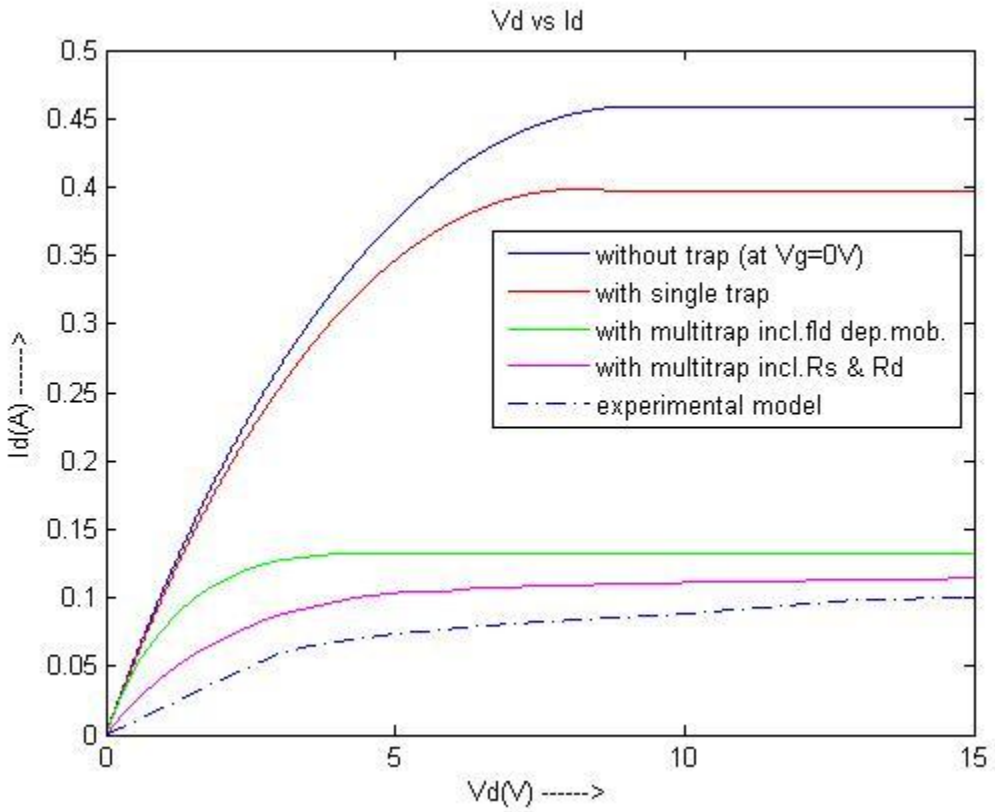

Figure 4.3: comparison of all I-V characteristics at different condition with experimental model

4.5.2 Summary

So by including source and drain resistance with three different trap concentration in our model, we get much close to experimental result (pink color) with good accuracy.

4.6 Self heating effect on I-V characteristics of 4H-SiC MESFETs (Detrapping)

The self-heating effect is well-known in microwave devices and plays a important role in the detrapping of captured carriers by various traps. The detrapping of the captured electrons is initiated with increasing negative gate voltage and the channel electron concentration increases which is accelerated by increased thermal effects. As a result, restoration of collapsed drain current is obtained before the trapping effect is maintained at high drain bias. The variation of the saturation velocity with channel temperature has a significant effect on the I–V characteristics in the saturation region.

4.6.1 Analytical model for self heating effect

Increasing temperature mainly effect mobility, intrinsic carrier concentration, emission rates of hole and electron.

a. mobility

$$\mu = \mu_o \left(\frac{T}{300}\right)^{-2.25} \tag{4.15}$$

where μ_o is low field electron mobility

b. intrinsic carrier concentration

$$n_i = (N_c . N_v)^{0.5} . e^{\left(\frac{-E_g}{2KT}\right)} \tag{4.16}$$

c. emission rates of holes and electrons.

$$e_{p/n} = \sigma_{p/n} . v_{p/n} . N_{v/c} exp\left(\frac{-\Delta E}{KT}\right) \tag{4.17}$$

d. Energy Fermi level.

4.6.2 Experimental Evaluation and Simulation Result

Some parameter value which is affected by changing temp used in simulation of self heating effect of 4H-SiC MESFET at different Temperature which is shown in table.

Table 4.3: Parameter value used in simulation at temp 300k and 500k

Parameter name	**@ Temp=300 k**	**@ Temp=500 k**
mobility	560 $cm^2/v-sec$	177 $cm^2/v-sec$
Intrinsic carrier conc.	$1.03x10^{-8}\ cm^{-3}$	578 cm^{-3}
Built in potential	1.5 V	1.4367 V
Fermi level (from conduction band)	0.91 eV	0.75 eV

Table 4.4: Emission rates of electron and holes of different trap at temp 300k and 500k

Name of Trap	**@ T=300k**	**@ T=500k**
$Z_{1/2}$	e_n=0.2516/cm^3-sec e_p=0.08	e_n =7.92x10^3 e_p =2.52x10^3
$RD_{1/2}$	e_n =2.72x10^{-6} e_p =9.9x10^{-10}	e_n =4.7697 e_p =.0017
$EH_{6/7}$	e_n =1.07x10^{-16} e_p =8.15x10^{-20}	e_n =1.28x10^{-5} e_p =9.74x10^{-9}

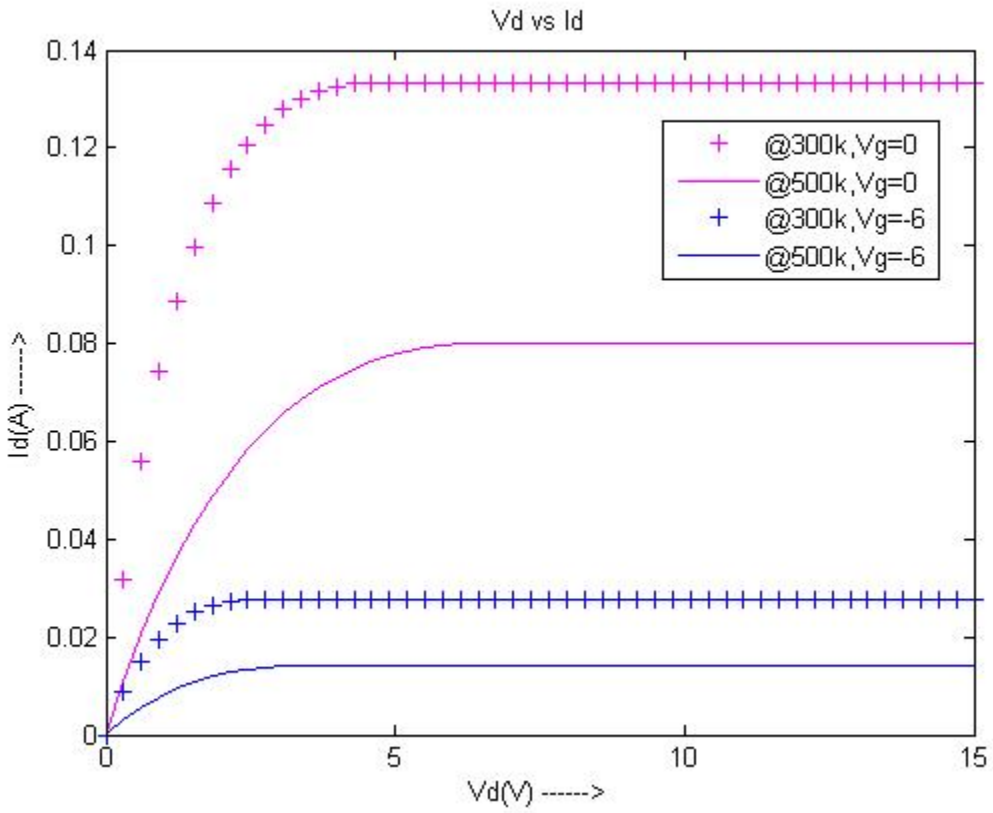

Figure 4.4: Comparision of I-V characteristics at V_g=0V (pink colour) & V_g= -6V (blue colour) of I_D(300k, 500k) resp.

4.7 Normalized drain current

It is the ratio of drain current at particular gate voltage. In this simulation, ratio of drain current at 300 k and at 500 k is taken which shows the variation of drain current by increasing drain voltage at particular gate voltage.

$$I_{norm} = \frac{I_D \text{ @ } 300\ k}{I_D \text{ @ } 500\ k}$$

4.7.1 Simulation Result

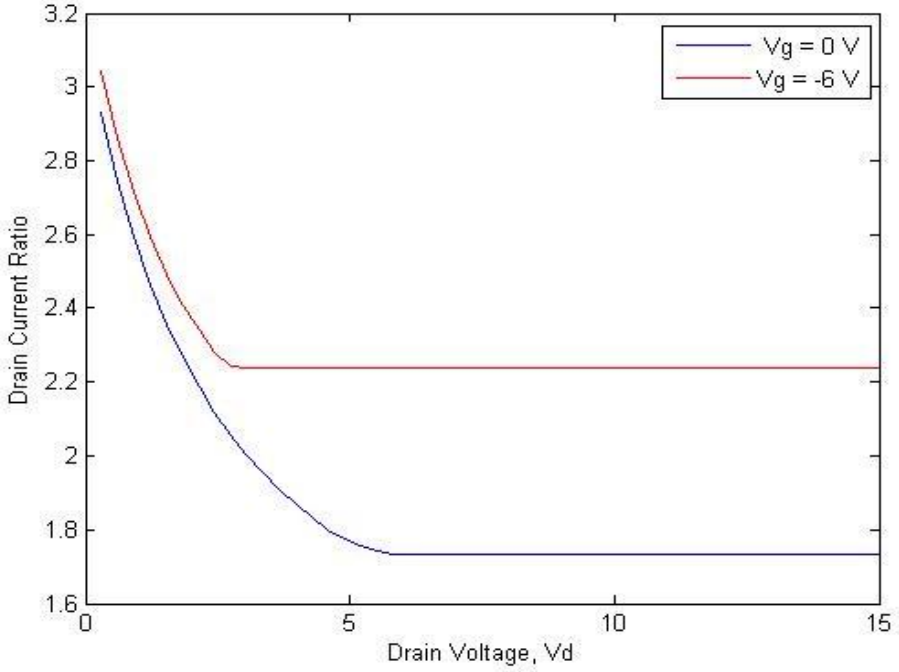

Figure 4.5: Normalized drain current (normalized by dividing I_{300k} with I_{500k}) at V_g=0V and it is compared with normalized current at V_g= -6 V

4.7.2 Summary

In this, we simulate the model at different temperature 300k and 500k. First there is simulation at V_g = 0V for both temperature. There we can see that as we increase the temperature from 300k to 500k, there is reduction of large amount of drain current. But when we simulate model by increasing gate voltage to -6 V for both temperature, there is reduction of drain current but by very less amount. It means that by increasing gate voltage at higher temperature, the trapped electron is detrapped into channel and again involved in producing drain current.

In next simulation plot, there is clear view of normalized drain current in which drain current is reducing by increasing drain voltage in linear region but in the case of zero gate voltage more current is reducing in comparision of V_g = -6 V.

Chapter 5

Conclusion and future scope of work

5.1 Introduction

Silicon carbide (SiC) based semiconductor electronic devices and circuits are presently being developed for high-frequency, high-power, and high-temperature applications because of its excellent properties such as wide band gap, high breakdown voltage, high thermal conductivity, and high saturation electron drift velocity. But One prominent issue is the effect of traps on the device which degraded the microwave power performance.

An analytically based model of 4H-SiC MESFETs including trapping and self-heating effects is developed. Then we explained the trapping process with the help of multi deep level trap by including various trap parameters like trap concentration, substrate concentration etc. source and drain resistance also played very important role for reducing of drain current. After that the detrapping process is also explained by increasing temperature at high drain voltage which is shown in chapter 2-4. Finally, we have discussed the scope of further research works which may be carried out in the near future.

5.2 Summary and conclusions

In **Chapter-1,** an overview of 4H-SiC MESFET is explained briefly. Firstly all general properties of 4H-SiC MESFET is explained. The advantage of 4H-SiC electronics technology are highlighted.. Then in this chapter, there is brief description about MESFET including principle of operation. $I_D\ (V_D, V_g)$ Characteristics of MESFET are compared at different condition. It has been also observed that the semi-insulating nature of substrate is affected by

many defects such as trap effects as we know that trapping effects play a significant role in the performance observed in 4H-SiC MESFET. Then a detailed literature review on the work of 4H-SiC MESFET including trapping effect of many author has been presented.

In **chapter-2,** just a theoretical model has been presented in both linear and saturation region without taking any trap parameter bye sze's model to fulfill the accuracy of basic 4H-SiC MESFET operation. And the simulation result confirmed the accurate model of I-V characteristics which are in good agreement with basic I-V characteristics of MESFET operation.

In **chapter-3,** a new analytical model of I-V characteristics of 4H-SiC MESFET including single trap level in both linear and saturation region has been proposed. A new expression for drain current is presented including trap concentration. In this chapter, it is shown that drain current in the channel is reduced due to trap of electron in the substrate from channel.

In **chapter-4,** An Improved I-V Model of 4H-SiC MESFETs with Multiple Deep Level Traps (DLT) and self heating effect has been proposed. In this, three different type of trap is presented. The simulated results have been compared with the reported experimental results by combining all three trap concentration with field dependent mobility, source and drain resistance, channel length modulation. The modeled results have closely tracked the experimental results reported in literature.

5.3 Future scope of work

While analyzing the model presented in this thesis, we have neglected the effect of surface states between the gate-source and gate-drain openings of the 4H-SiC MESFET throughout. Due to this a depletion region forms at the gate-source and gate-drain openings, by which the value of source and drain current become larger than previous value. As a result of this we can get I-V characteristics much more close to experimental result or may be with full accuracy.

This thesis has been focused on modeling the dc and microwave characteristics of 4H-SiC MESFET for both the linear and saturation regions including multi deep level traps. So one may extend this work by taking ac characteristics (frequency dispersion) into account.

Then buffer layer is also neglected between channel and substrate in this thesis, so this work can be extended by taking buffer layer into account. Finally there is still some important work in this topic which can be taken up as future work to improve the model of 4H-SiC MESFET.

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